

BLA0912-250

Avionics LDMOS transistor

Rev. 02 — 22 July 2004

Product data sheet

1. Product profile

1.1 General description

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead SOT502A flange package with a ceramic cap. The common source is connected to the mounting flange.

1.2 Features

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

1.3 Applications

- Avionics transmitter applications in the 960 MHz to 1215 MHz frequency range such as Mode-S, TCAS and JTIDS, DME or TACAN.

1.4 Quick reference data

Table 1: Quick reference data

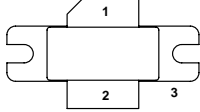
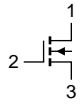
Typical RF performance measured in common source class-AB circuit at $P_L = 250\text{ W}$ and 960 MHz to 1215 MHz frequency band. $T_h = 25\text{ °C}$; $Z_{th} = 0.15\text{ K/W}$; unless specified otherwise.

Mode of operation	Conditions	V_{DS} (V)	P_L (W)	G_p (dB)	ΔG_p (dB)	η_D (%)	Pulse droop (dB)	t_r (ns)	t_f (ns)	$Z_{th(j-h)}$ (K/W)	φ_R (deg)
All modes	$t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$	36	250	13.5	0.8	50	0.1	25	6	0.18	± 5
TCAS: 1030 MHz to 1090 MHz	$t_p = 32\text{ }\mu\text{s}$; $\delta = 0.1\text{ }\%$	36	250	14.0	0.8	50	0	25	6	0.07	± 5
Mode-S: 1030 MHz to 1090 MHz	$t_p = 128\text{ }\mu\text{s}$; $\delta = 2\text{ }\%$ $t_p = 340\text{ }\mu\text{s}$; $\delta = 1\text{ }\%$	36	250	13.5	0.8	50	0.1	25	6	0.15	± 5
JTIDS: 960 MHz to 1215 MHz	$t_p = 3.3\text{ ms}$; $\delta = 22\text{ }\%$	36	200	13.0	1.2	45	0.2	25	6	0.45	± 5

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2. Pinning information

Table 2: Pinning

Pin	Description	Simplified outline	Symbol
1	drain	 <p>Top view</p>	 <p>sym039</p>
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 3: Ordering information

Type number	Package		
	Name	Description	Version
BLA0912-250	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A

4. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	75	V
V_{GS}	gate-source voltage (DC)		-	± 22	V
P_{tot}	total power dissipation	$T_h \leq 25\text{ °C}$; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\%$	-	700	W
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-h)}$	thermal impedance from junction to heatsink	$T_h = 25\text{ °C}$	[1] 0.18	K/W

[1] Thermal resistance is determined under RF operating conditions; $t_p = 100\text{ }\mu\text{s}$, $\delta = 10\%$.

6. Characteristics

Table 6: Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 3\text{ mA}$	75	-	-	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 300\text{ mA}$	4	-	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 36\text{ V}$	-	-	1	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9\text{ V}; V_{DS} = 10\text{ V}$	45	-	-	A
I_{GSS}	gate-source leakage current	$V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}$	-	-	1	μA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 10\text{ A}$	-	9	-	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = 9\text{ V}; I_D = 10\text{ A}$	-	60	-	$\text{m}\Omega$

7. Application information

Table 7: Application information

RF performance in common source class-AB circuit; $T_h = 25\text{ }^\circ\text{C}$; $Z_{th} = 0.15\text{ K/W}$; unless specified otherwise.

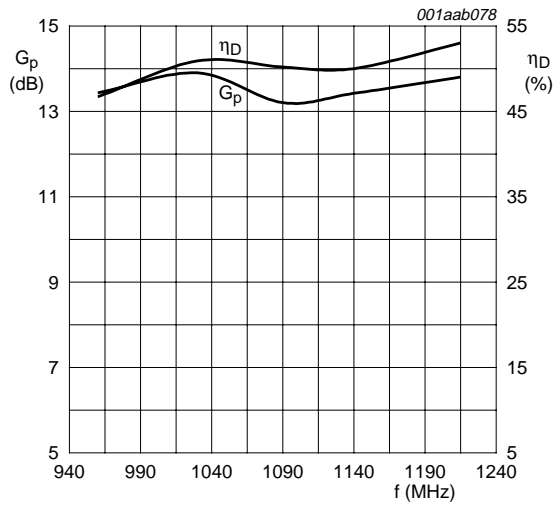
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage		-	-	36	V
f	frequency		960	-	1215	MHz
P_L	load power	$t_p = 100\text{ }\mu\text{s}; \delta = 10\%$	250	-	-	W
G_p	power gain	$P_{OUT} = 250\text{ W}$	12	13	-	dB
η_D	drain efficiency	$t_p = 100\text{ }\mu\text{s}; \delta = 10\%$	40	50	-	%
Z_{th}	thermal impedance	$t_p = 100\text{ }\mu\text{s}; \delta = 10\%$	-	-	0.2	K/W
t_r	rise time		-	25	50	ns
t_f	fall time		-	6	25	ns
	pulse droop	$t_p = 100\text{ }\mu\text{s}; \delta = 10\%$	-	0.1	0.5	dB
	spurious	$V_{SWR_L} = 2:1$	-	-	-60	dBc
T_h	heatsink temperature		-55	-	+70	$^\circ\text{C}$

7.1 Ruggedness in class-AB operation

The BLA0912-250 is capable of withstanding a load mismatch corresponding to VSWR = 5:1 through all phases under the following conditions: $V_{DS} = 36\text{ V}$; $f = 960\text{ MHz}$ to 1215 MHz at rated load power.

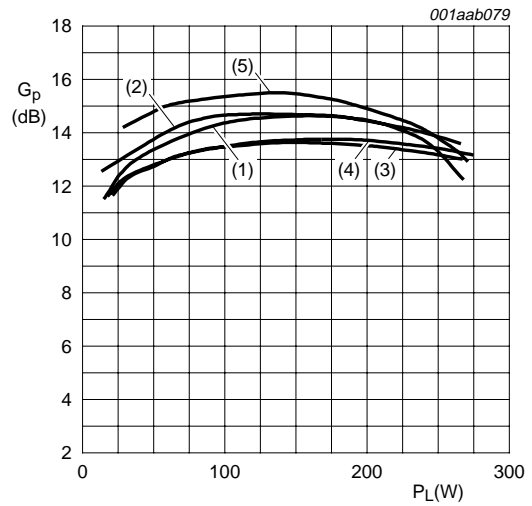
Table 8: Typical impedance values

Frequency (MHz)	$Z_S (\Omega)$	$Z_L (\Omega)$
960	$0.89 - j1.70$	$1.53 - j1.13$
1030	$1.37 - j1.23$	$1.47 - j0.99$
1090	$2.09 - j1.27$	$1.38 - j0.85$
1140	$2.40 - j1.97$	$1.30 - j0.71$
1215	$1.51 - j2.61$	$1.17 - j0.47$



$T_h = 25\text{ }^\circ\text{C}$; $V_{DS} = 36\text{ V}$; $I_{DQ} = 150\text{ mA}$; class-AB;
 $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$.

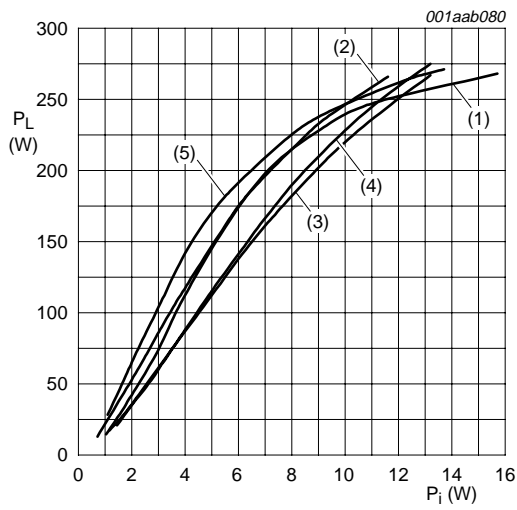
Fig 1. Power gain and drain efficiency as function of frequency; typical values.



$T_h = 25\text{ }^\circ\text{C}$; $V_{DS} = 36\text{ V}$; $I_{DQ} = 150\text{ mA}$; class-AB;
 $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$.

- (1) $f = 960\text{ MHz}$.
- (2) $f = 1030\text{ MHz}$.
- (3) $f = 1090\text{ MHz}$.
- (4) $f = 1140\text{ MHz}$.
- (5) $f = 1215\text{ MHz}$.

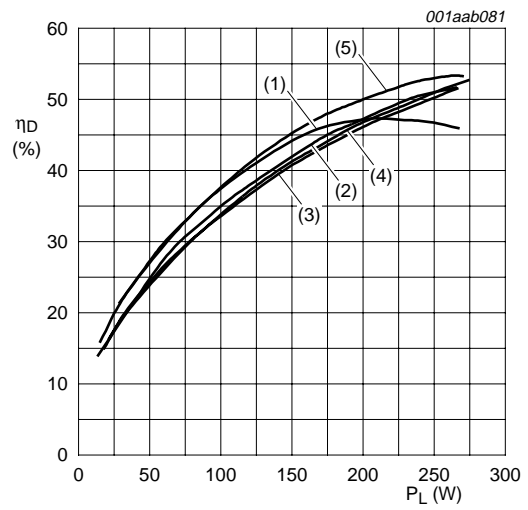
Fig 2. Power gain as function of load power; typical values.



$T_h = 25\text{ }^\circ\text{C}$; $V_{DS} = 36\text{ V}$; $I_{DQ} = 150\text{ mA}$; class-AB;
 $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ \%}$.

- (1) $f = 960\text{ MHz}$.
- (2) $f = 1030\text{ MHz}$.
- (3) $f = 1090\text{ MHz}$.
- (4) $f = 1140\text{ MHz}$.
- (5) $f = 1215\text{ MHz}$.

Fig 3. Load power as function of input power; typical values.



$T_h = 25\text{ }^\circ\text{C}$; $V_{DS} = 36\text{ V}$; $I_{DQ} = 150\text{ mA}$; class-AB;
 $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ \%}$.

- (1) $f = 960\text{ MHz}$.
- (2) $f = 1030\text{ MHz}$.
- (3) $f = 1090\text{ MHz}$.
- (4) $f = 1140\text{ MHz}$.
- (5) $f = 1215\text{ MHz}$.

Fig 4. Efficiency as function of load power; typical values.

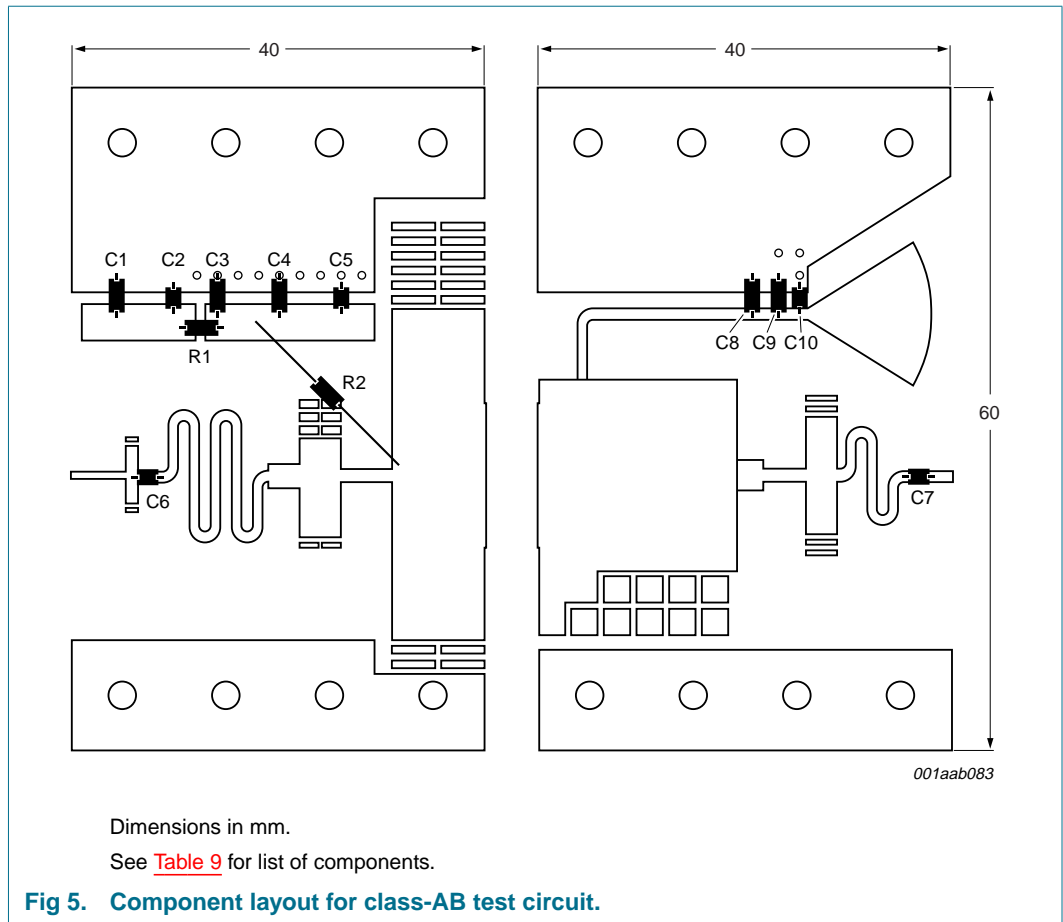


Table 9: List of components for class-AB test circuit (see [Figure 5](#)). [1]

Component	Description	Value	Catalogue no.
C1	multilayer ceramic chip capacitor	1 nF	[3]
C2	multilayer ceramic chip capacitor	22 pF	[2]
C3	multilayer ceramic chip capacitor	1 nF	[3]
C4	KEMET tantalum SMD capacitor	47 μ F	T491D476M020AS
C5	multilayer ceramic chip capacitor	56 pF	[2]
C6	multilayer ceramic chip capacitor	22 pF	[2]
C7	multilayer ceramic chip capacitor	47 pF	[2]
C8	KEMET tantalum SMD capacitor	22 μ F	T491D226M020AS
C9	multilayer ceramic chip capacitor	1 nF	[3]
C10	multilayer ceramic chip capacitor	22 pF	[2]
R1	SMD resistor (0805)	51 Ω	
R2	philips resistor	49.9 Ω	2333 156 14999

[1] Layout files are available on request in gerber and dxf format.

[2] American Technical Ceramics type 100A or capacitor of same quality.

[3] American Technical Ceramics type 100B or capacitor of same quality.

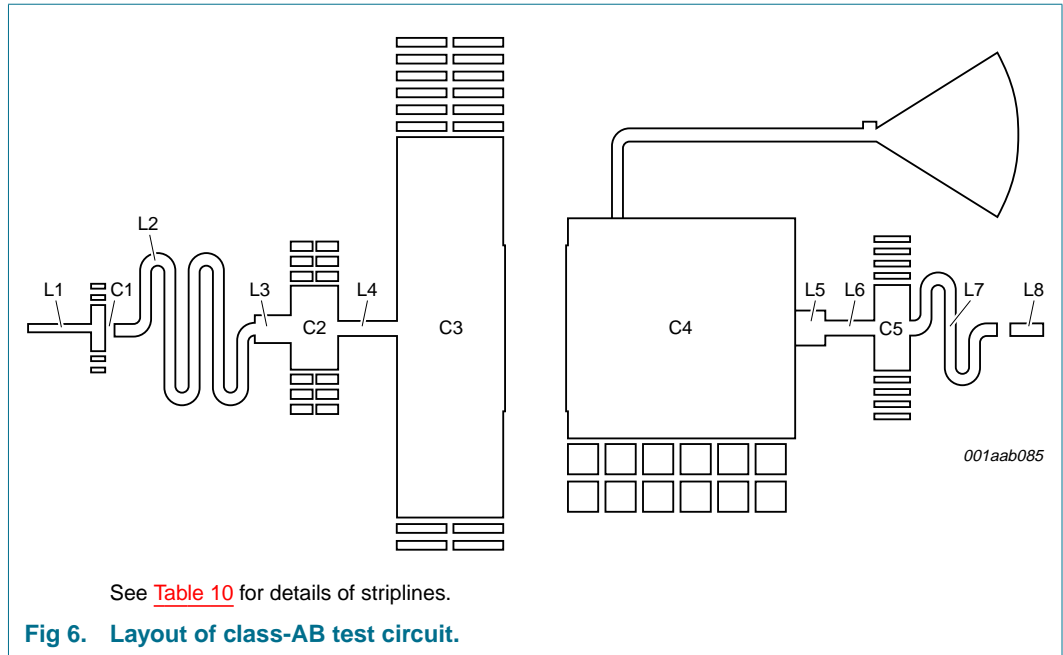


Table 10: Layout details for class-AB test circuit (see [Figure 6](#)). [1]

Component	Description	Dimensions
Input circuit		
L1	stripline	5 mm × 0.8 mm
C1	stripline	1.2 mm × 3.5 mm
L2	stripline	cap. pad: 1 mm × 1 mm (1×) curve: width 0.8 mm; angle 90°; radius 0.8 mm (10×) vertical: 3.9 mm × 0.8 mm (2×) vertical: 9.4 mm × 0.8 mm (3×) horizontal: 0.5 mm × 0.8 mm (4×)
L3	stripline	3 mm × 2 mm
C2	stripline	4 mm × 6.5 mm
L4	stripline	5 mm × 1 mm
C3	stripline	8.8 mm × 30 mm + 0.2 mm × 13 mm
Output circuit		
C4	stripline	0.2 mm × 13 mm + 19 mm × 17.1 mm
L5	stripline	2.5 mm × 2.3 mm
L6	stripline	4 mm × 1 mm
C5	stripline	3 mm × 6.6 mm
L7	stripline	curve: width 0.8 mm; angle 90°; radius 0.8 mm (6×) vertical: 2.2 mm × 0.8 mm (2×) vertical: 6 mm × 0.8 mm (1×) horizontal: 1 mm × 0.8 mm (2×)
L8	stripline	2.5 mm × 0.8 mm

Table 10: Layout details for class-AB test circuit (see Figure 6). [1] ...continued

Component	Description	Dimensions
1/4 λ line	stripline	curve: width 1 mm; angle 90°; radius 0.8 mm
		vertical: 5 mm \times 1 mm
		horizontal: 19 mm \times 1 mm
		tapered line: $W_1 = 1$ mm; $L = 12$ mm; angle = 60°

[1] Striplines are on a Rogers Duroid 6010 printed-circuit board ($\epsilon_r = 10.2$); thickness = 0.64 mm.

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

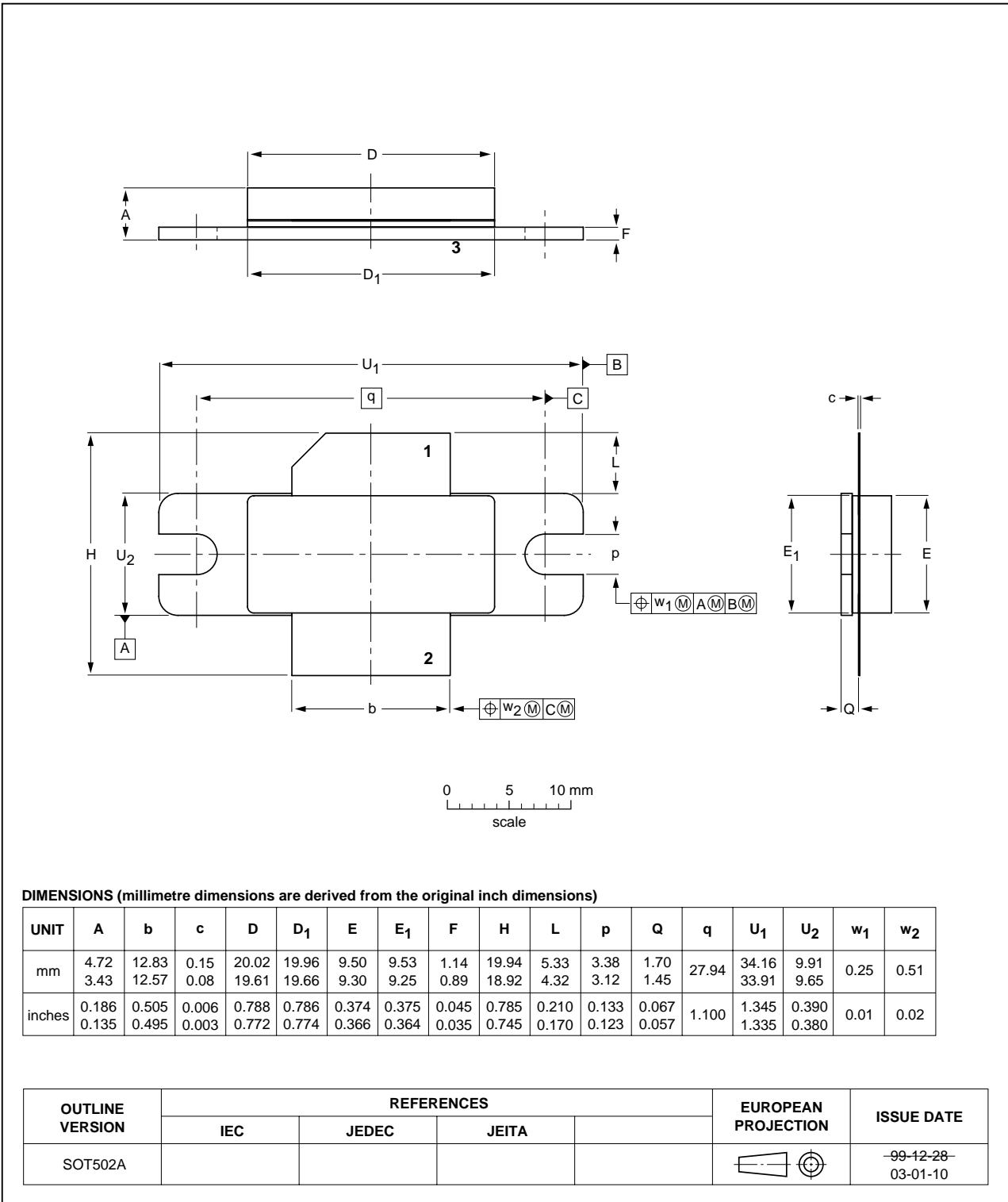


Fig 7. Package outline.



9. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
BLA0912-250_2	20040722	Product data	-	9397 750 13275	BLA0912-250_N_1
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.				
BLA0912-250_N_1	20031024	Preliminary specification	-	9397 750 12224	-

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^[2] ^[3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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